REMARKS

This Amendment is filed in response to the Office Action dated December 16, 2005. For the following reasons this application should be allowed and the case passed to issue. No new matter is introduced by this amendment. The amendment to claim 13 and new claims 19 and 20 are supported by the fourth embodiment in the specification (page 11, line 25 to page 12, line 13 and Fig. 5).

Claims 1-13 and 16-20 are pending in this application. Claims 1-12 have been withdrawn pursuant to a restriction requirement. Claims 13 and 16-18 have been rejected. Claim 13 is amended in this response. New claims 19 and 20 are added. Claims 14 and 15 were previously canceled.

Claim Rejections Under 35 U.S.C. § 103

Claims 13 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashi (JP 6-318561) in view of Kanekawa et al. (U.S. Pat. No. 6,624,474) and Hayashi (U.S. Pub. Pat. App. No. 2003/0232490). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 13, is a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a well region of a semiconductor layer. Each semiconductor element has a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between the source and the drain, and a drift layer of the first-conductivity-type in an upper region the well region. The method comprises the steps of implanting impurities concurrently into a first drift layer of one semiconductor element and into

a second drift layer of another semiconductor element. An implantation mask is used that includes a portion corresponding to the first drift layer of the one semiconductor element and has a first opening ratio as well as a portion corresponding to the second drift layer of the another semiconductor element and has a second opening ratio different from the first opening ratio. The one semiconductor element has a breakdown voltage higher than that of the another semiconductor element. The implantation mask used has the first opening ratio smaller than the second opening ratio. The one semiconductor element is adjacent to the another semiconductor element. A wall-shaped element-isolation insulating film for isolating the one semiconductor element from the another semiconductor element is provided in the semiconductor layer prior to the step of implanting impurities. The integrated semiconductor device is annealed after the step of implanting impurities to diffuse the impurities.

The Examiner asserted that Hayashi (`561) (Figs. 1-4) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources and drains, and implanting impurities through an implantation mask having different opening ratios (A, A'). The Examiner further asserted that Hayashi (`561) discloses that the semiconductor elements have different breakdown voltages. The Examiner acknowledged that Hayashi (`561) lacked anticipation of a wall-shaped element isolation insulating film for isolating one semiconductor element from another semiconductor element prior to the step of implanting impurities. The Examiner averred that Kanekawa et al. disclose a method of manufacturing an integrated semiconductor device having a plurality of elements and a wall-shaped element-isolation film 4/101 for isolating the semiconductor elements. The Examiner further alleged that Hayashi (`490) teaches a wall-shaped isolation film for isolating one semiconductor element from another. The Examiner concluded that one of ordinary skill in the

art would have been motivated to incorporate a wall-shaped element isolation film to ensure isolation of the semiconductor elements. The Examiner acknowledged the combined references are silent regarding providing the wall-shaped element-isolation insulating film prior to implanting the impurities. However, the Examiner concluded that it would have been obvious to form isolation walls prior to implanting impurities so as to protect device elements from each other.

The combination of Hayashi ('561), Kanekawa et al., and Hayashi ('490), however, does not suggest the claimed method of manufacturing an integrated semiconductor device. The cited references whether taken alone, or in combination, do not suggest a method of manufacturing an integrated semiconductor device including a drift layer of the first-conductivity-type in an upper region of the well region comprising the steps of implanting impurities concurrently into a first drift layer of the one semiconductor element and into a second drift layer of another semiconductor element, using an implantation mask that includes a portion corresponding to the first drift layer of said one semiconductor element and having a first opening ratio as well as a portion corresponding to the second drift layer of the another semiconductor element and having a second opening ratio different from the first opening ratio, as required by claim 13. The cited references do not suggest forming the drift layers required by claim 13.

As disclosed in the specification (page 12, lines 3-13) the drift layers provided in the upper region of the well region allow the flow of electric current to be linear. A resultant effect is that the on resistance of the integrated semiconductor device can be lowered.

Claims 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashi ('561) in view of Kanekawa et al. and Hayashi ('490) and further in view of Yoshida

(JP 6-312918). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

The Examiner acknowledged that Hayashi ('561), Kanekawa et al., and Hayashi ('490) do not disclose the mesh implantation masks having dot-like openings. The Examiner asserted that Yoshida teaches mesh implantation or dot implantation masks and concluded that it would have been obvious to incorporate Yoshida's teaching to enable regions having different concentrations to be formed in a single process.

Claims 17 and 18 are allowable for at least the same reasons as claim 13, as Yoshida does not cure the above-noted deficiencies of Hayashi ('561), Kanekawa et al., and Hayashi ('490). Yoshida does not suggest forming the drift layers required by claim 13. In addition, Yoshida does not disclose the dot implantation mask, as required by claim 18.

The dependent claims are allowable for at least the same reasons as claim 13 and further distinguish the claimed invention. Likewise, new dependent claims 19 and 20 are allowable for at least the same reasons as claim 13 and further distinguish the claimed method of manufacturing an integrated semiconductor device. For example, claim 19 further requires that the impurity concentration of the drift layer is higher than the well region. Claim 20 further requires that the impurity concentration of the first drift layer is lower than the second drift layer.

In view of the above amendments and remarks, Applicants submit that this application should be allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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